I. Listing of Claims

1. (Previously Presented) A field-effect transistor with local source-drain insulation, having

a semiconductor substrate;

a source depression and a drain depression, which are formed in a manner spaced apart from one another in the semiconductor substrate;

a depression insulation layer, which is formed at least in a bottom region of the source depression and of the drain depression;

an electrically conductive filling layer, which is formed for realizing source and drain regions and for filling the source and drain depressions at a surface of the depression insulation layer;

a gate dielectric, which is formed at a substrate surface between the source and drain depressions; and

a gate layer, which is formed at a surface of the gate dielectric,

wherein the source and drain depressions have, in an upper region, a widening with a predetermined depth for realizing defined channel connection regions.

2. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein the depression insulation layer has a depression sidewall insulation layer, which is formed in a sidewall region of the source and drain depressions but does not touch the gate dielectric.

3. (Cancelled)

4. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein the electrically conductive filling layer has a seed layer for improving a deposition in the source and drain depressions.

5. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein a gate insulation layer is formed at sidewalls of the gate layer.

6. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein the field-effect transistor is bounded by shallow trench isolations.

7. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein the field-effect transistor has lateral structures < 100 nm.

8. (Previously Presented) The field-effect transistor as claimed in claim 1, wherein the source and drain depressions have a depth of approximately 50 nm to 300 nm.

9. (Previously Presented) The field-effect transistor as claimed in claim 2, wherein the depression sidewall insulation layer extends into a region below the gate dielectric.

10-21. (Cancelled)